

CRATON product brief

CRATON⁽¹⁾ is an integrated vehicular communication processor. CRATON provides the highest communication and safety decision reliability, while minimizing the required system external components. CRATON contains the complete functionality required by a vehicular communication safety solution complemented by Autotalks' PLUTON RF device.

CRATON optimizes all the required functionality of a vehicular communication processor. The high integration level boosts the performance by applying cross-layer design techniques. Side information from one layer assists with the operation of another layer.

CRATON-G also integrates optimized GNSS Baseband receiver for Vehicle-to-Vehicle applications. CRATON-G incorporates connectivity to a low-cost, low-footprint, external GNSS Radio, for a complete positioning system.

Features

CRATON supports the following features:

- On-board Unit (OBU) operation, Road-side Unit (RSU) operation
- Worldwide standards-compliant operation:
 - IEEE802.11p
 - US IEEE1609
 - Japan ARIB T-109
 - European ETSI ITS
- Supports OEM integrated and after-market unit operation
- Supports 802.11a WiFi operation, Client and AP modes
- 240MHz⁽²⁾ ARM Cortex R4F with ECC-protected 32KB data cache, 32KB instruction cache and a floating point unit
- Two 240MHz⁽²⁾ ARC 625D RISC controllers with 8KB data cache, 8KB instruction cache and a DSP unit
- High-performance **GuaranteedMobility™** modem optimized for vehicular operation
- Line-rate elliptic cryptography **GuaranteedSecurity™** co-processor
- **GuaranteedDelivery™** intersection congestion avoidance
- Generic congestion control algorithm
- **GuaranteedAccuracy™** relative positioning measurement
- Dual PHY and MAC for Concurrent Control Channel (CCH) and Service Channel (SCH) operation
- MAC TDM operation for Japan R2V TDM operation

Notes:

1. CRATON's package markings include both Autotalks part number (ATK4100Ax) and Fujitsu Semiconductor part number (MB8AC2060). CRATON is manufactured using Fujitsu Semiconductor Automotive ASIC 65nm process, and therefore marked with Fujitsu Semiconductor's marking.
2. 360MHz or 240MHz in CRATON ATK4100A0.
3. ATK4100A0-G and ATK4100A1-G versions.
4. PBGA 27mm x 27mm package with 1.0mm pitch for ATK4100A0.



- 96KB on-die, memory-mapped, static RAM, with ECC protection per word
- 8-bit DDR3-800 memory interface
- 16-bit NOR/NAND Flash/SRAM interface
- Two integrated 10-bit IQ DACs and two 10-bit IQ ADCs for analog RF chip interface
- Flexible RF control interface, including dedicated, configurable RF SPI bus and configurable control signal timing
- Flexible antenna configurations that support a single antenna serving two channels or two diversified antennas serving a single channel
- 1PPS GPS input for channel synchronization from an external GPS
- Dual, parallel GPS front-end interface for concurrent GPS and GLONASS support⁽³⁾
- 1Kb one-time programming array for a secure configuration and identity storage
- Secure boot from a digitally signed firmware and tamper-resistant production device implemented in Boot ROM
- Flashing over serial interfaces for production flow
- Secure certificate storage
- Two CAN bus interfaces, compliant with CAN specification, Version 2.0 Part B
 - 10/100 half-/full-duplex Ethernet MII / RMI interface with 802.1 AVB support
- Two 921Kbit UART interfaces for external GPS, CPU control and other peripherals
- Five SPI interfaces, up to 20MHz Master/Slave operation
- I²C Master interface and I²S interface for stereo audio output
- On-die temperature sensor
- Four general-purpose timers and dedicated watchdog reset timer
- Two on-chip PLLs for DDR3 and SoC operation using a single clock input; FM-PLL for minimal EMI
- Auxiliary 500KHz – 20MHz clocks generation
- Low power consumption (< 1.33 W)
- PBGA 18mm x 18mm package with 0.8mm pitch⁽⁴⁾
- -40° to 85° ambient temperature operation range
- -55° to 125° storage temperature range
- Automotive grade AEC Q-100 grade 3 qualification path

1. Device Overview

ARM Cortex-R4F Core with L1 I/D-Cache

The Cortex-R4 processor is a mid-range processor for use in deeply embedded, realtime systems. It implements the ARMv7R architecture, and includes Thumb-2 technology for optimum code density and processing throughput. The pipeline has a single Arithmetic Logic Unit (ALU), but implements limited dual-issuing of instructions for efficient utilization of other resources, such as the register file.

Error Checking and Correction (ECC) is used on the Cortex-R4 in Level 1 (L1) memories to provide improved reliability and to address safety-critical applications.

Dual IEEE802.11P MAC and PHY (MAC-PHY)

CRATON includes implementation of two IEEE802.11P channels.

The two channels are fully autonomous, with separate PHY and MAC functionality. A single CRATON device can support two different channels (CCH and SCH), or a single channel (either CCH or SCH) with antenna diversity. The CRATON PHYs are optimized for vehicular conditions, which a traditional 802.11 PHY typically lacks.

The MACs are fully compliant to both IEEE802.11a/p and ARIB T109 standards.

Notable features of the PHY are:

- Ultrafast Channel Tracking – for reception from fast moving vehicles, and support for deep-fading channels, as commonly seen in Non-Line-Of-Sight (NLOS) environments.
- Enhanced Adjacent Channel Rejection – CRATON supersedes the IEEE802.11p specification by maintaining the 28dB rejection requirement for any input power. In real life, the input power varies and is not limited to a certain value.
- Optimized Packet Boundary Detection – patented scheme improving performance for both NLOS and LOS conditions.
- Transmission Mask C – for minimizing out-of-band emissions.
- PAPR Reduction - decreases the peak signal power, thereby increasing the average signal power without reaching the PA non-linear operation range.
- Diversity operation – Optimal receive diversity gain enables operation in difficult installation environments, such as in in-cabin aftermarket devices. Transmit diversity is implemented to provide a flat omnidirectional radiation pattern when the two antennas transmit concurrently.
- Automatic Noise-level Detection – for lowest sensitivity at vehicular environment

Analog-to-digital I/Q Converters

CRATON includes on-die differential analog-to-digital converters capable of delivering 40 Mega Samples per Second in 10-bit resolution. There are two instances of these converters, each per I/Q pair (channel), totaling 20 bits per instance.

Digital-to-analog I/Q Converters

CRATON includes on-die differential digital-to-analog converters capable of delivering 40 MSPS in 10-bit resolution. There are four instances of these converters, each per I or Q signal, totaling 10 bits per instance. Each pair of those converters is bias-matched, servicing one I/Q pair (channel).

RF Control Serial Peripheral Interfaces (RFSPI)

The CRATON has two RF SPI channels operating as SPI masters that are used for RFIC control, complemented with four discrete RF control output signals per channel. The RF SPI timing is controlled by a Generic RFIC Interface (GRFI) module. The GRFI is intended to provide the CRATON chip with the widest possible selection range for RF submodule components, given its flexible mechanism for converting its hardware needs into SPI and dedicated IO transactions. GRFI is purposely made to work with Autotalks' PLUTON RFIC, with a maximum clock frequency of 40 MHz

Multi-protocol Multi-layer Bus Matrix (MATRIX)

CRATON implements a high-performance multi-layer bus matrix that connects the various components of the SoC. The bus matrix communicates with master and slave entities, based on AMBA AXI, AHB or APB bus standards, to achieve optimal balance of performance vs. footprint.

DMA Controller (HDMAC)

CRATON implements an eight-channel AMBA AHB DMA Controller for copying data without CPU intervention.

General-purpose SRAM (GPRAM)

CRATON implements 96 KB of on-die, memory-mapped, static RAM. The memory array is accessible by all bus masters in the SoC. Each 32-bit word is protected by a seven-bit ECC signature for improved reliability. Optional detection and/or correction of ECC errors. ECC codes can detect up to two bit errors, and correct up to one bit error per word.

Security RISC Controller (SEC_ARC)

ARC625D RISC Processor core serves as security controller.

Elliptic Curve Crypto Accelerator (ECC)

CRATON implements a high-performance Elliptic Curve Cryptography subsystem, to allow 802.11p line rate verification to support all use cases of vehicle-to-vehicle or infrastructure-to-vehicle communication. The subsystem is implemented by three identical hardware acceleration engines, capable of extremely fast ECDSA256 verification operations, each in less than 2 mS. The subsystem also supports ECDSA Sign and ECIES (IEEE1363a) operations with flexibility to support other algorithms as required.

SHA2/HMAC Hash Engine (SHA2)

The CRATON SHA2 secure hash processor is a compact, high-performance, low-power processor that implements the secure hash algorithms (SHA-1, SHA-224, SHA-256, SHA-384 and SHA-512) defined by FIPS 180-2.

True Random Number Generator (RNG)

The CRATON RNG is a high-performance random number generator (RNG) that combines a non-deterministic RNG with a non-linear deterministic RNG. The CRATON RNG meets FIPS 140-1 requirements.

GNSS Baseband RISC Controller (GNSS_ARC)

ARC625D RISC Processor core serves as the GNSS Baseband RISC Controller. It includes 8KB data cache and 8KB instruction cache, and 4KB of closely coupled data memory. 16KB DSP Memory subsystem is embedded, allowing auto-increment operations for common DSP functions, like FFTs, with customized DSP instructions.

GPS/GLONASS Correlation Engine (GNAC)

The GNAC module is a hardware accelerator that processes the signals received from GPS/GLONASS satellites in order to offload and improve performance of the GNSS subsystem. Full positioning/navigation processing takes place using GNSS software running on the CRATON ARC625D GNSS RISC Controller.

Static Memory Controller (MEMCS)

The Static Memory Controller (MEMCS) generates the signals that control the access to the external memory devices or peripheral devices. It has three chip selects and a 24-bit address bus. The 16-bit data bus can be configured to interface with 8-bit or 16-bit external devices. Separate read and write control signals allow direct memory and peripheral interfacing.

Vectored Interrupt Controller and IRQ Subsystem (VIC)

The CRATON Vectored Interrupt Controller, VIC, handles the internal interrupts asserted by different sources, according to configurable priority and mask registers, and forwards the selected interrupt to the CPU along with interrupt jump addresses.

Timers

The CRATON Timers module consists of two programmable 32-/16-bit down counters that can generate interrupts upon reaching zero.

Watchdog

The CRATON Watchdog module is a 32-bit counter-based module initialized by a reload register. The Watchdog module applies a reset to the system in the event of a software failure, thereby providing a way to recover from software crashes. The Watchdog unit can be enabled or disabled, as required.

Universal Asynchronous Receivers Transmitters (UART)

CRATON implements two UART interfaces, accessible via either polling or an interrupt scheme, with optional DMA operations.

Serial Peripheral Interfaces (SPIs)

CRATON has five SPI controllers that can operate as a master or a slave. Two SPI controllers support up to 20 Mbps. The other three SPI controllers support up to 10 Mbps.

Each controller supports either slave or master modes, in the one of the following modes of operation:

- A Motorola SPI-compatible interface
- A Texas Instruments synchronous serial interface
- A National Semiconductor Microwire interface

MII/RMII Ethernet MAC with Dedicated DMA

The CRATON implements an MII / RMII Ethernet MAC core compiling with IEEE 802.3 specifications. The MII/RMII Ethernet MAC can be configured to operate in either in Half-/Full-duplex mode, using 10/100Mbps data transfer rates and with or without an Auto-negotiation mechanism. The Ethernet MAC implements an internal DMA for transmit and receive data exchanges.

Controller Area Network Controllers (CAN)

CRATON implements two CAN controllers, compliant with the CAN Specification, Version 2.0 Part B. The CAN Controller features a programmable bit rate, as well as 15 message buffers, each configurable for transmit or receive. Programmable acceptance filtering provides support for both Full-CAN and Basic-CAN operation.

The CAN Controller control registers provide CPU control of bit rates, diagnostic functions, enabling/disabling the CAN Controller, CAN pin logic level, CAN bit time partitioning, incoming message filtering, transmit message prioritization and enabling/disabling interrupts. Status registers provide CAN node, interrupt and error/diagnostic status.

Inter-integrated Circuit Interface (I2C)

The CRATON I²C Interface provides full support for the two-wire I²C synchronous serial interface. The I²C serial interface consists of the standard bidirectional I²C signals: Serial Clock Line (SCL) and Serial Data Line (SDA). The CRATON I²C operates in Master mode only.

Inter-integrated Sound (I2S) Interface

The I²S audio interface provides a bidirectional, synchronous, serial interface to off-chip audio devices. It complies with the Inter-IC Sound (I²S) bus specification from Philips Semiconductor. The CRATON I²S interface can be driven either by interrupt or through the DMA to reduce CPU utilization. The CRATON I²S works in Master mode.

Temperature Sensor

The CRATON includes an on-die temperature sensor. The temperature sensor covers the range of -40°C to +125°C with +/- 10°C accuracy.

General-purpose Analog-to-digital Converter

The CRATON General-purpose Analog-to-digital Converter has maximum conversion rate: 1 MS/s, 10-bit resolution.

General Purpose IO (GPIO)

CRATON support 32 General Purpose IOs. Each GPIO can be either configured as an input or an output. GPIO interrupt event generation according configuration.

2. Pinout and Package

CRATON is packaged in PBGA 441 18 mm x 18 mm, 0.8mm pitch.

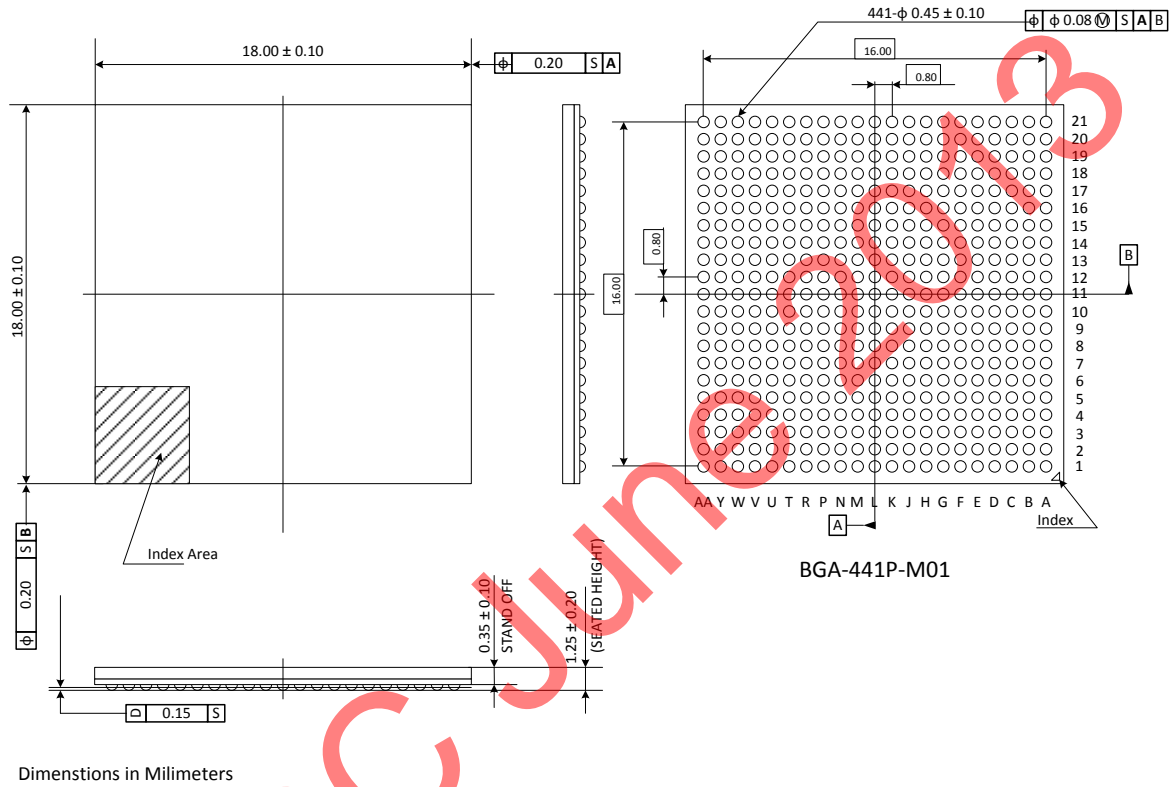


Figure 1: ATK4100A1 Package Outline Drawing



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